Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Previously presented) In a digital intermediate frequency downconversion circuit for downconverting in-phase and quadrature signal components of a digitized communication signal, a method for processing the in-phase and quadrature signal components of the digitized communication signal comprising:

processing a single serial digital bit stream formed of the in-phase and quadrature signal components of the digitized communication signal through a set of simple logic to produce a digital representation of downconverted in-phase and quadrature components; and

recombining the digital representation of the downconverted in-phase and quadrature components with a reconstruction filter in a manner to obtain a baseband signal substantially free of image artifacts.

2. (Previously presented) The method according to claim 1 further including the steps of:

employing an oversampled digital word of four bits in length from a source digital oscillator as a reference signal;

supplying digital signal mixers with said reference signal to achieve at least sixteen levels of accuracy as a sine wave mixing signal without significant phase or amplitude error;

mixing the digitized serial bit stream according to a clock with output of a four-bit wide table representing the reference signal;

recombining digitally the in-phase and quadrature signals to obtain a digitally combined signal; and

binary weighting the combined signal into a digital reconstruction filter to produce a downconverted signal that is unaffected by resistor tolerance.

3. (Original) In a digital IF downconversion circuit for downconverting in-phase and quadrature signal components of a digitized communication signal, a processor for in-phase and quadrature signal components of the digital signal comprising:

logic for processing a single serial digital bit stream formed of the in-phase and quadrature signal components to produce a digital representation of downconverted in-phase and quadrature components; and

a digital reconstruction filter for recombining the digital representation of the downconverted in-phase and quadrature components in a manner to obtain a digital representation of a baseband signal substantially free of image artifacts.

4. (Original) The circuit according to claim 3 further including:

a source digital oscillator supplying digital signal mixers with an oversampled digital word of four bits in length to achieve at least sixteen levels of accuracy for a sine wave mixing signal without significant phase or amplitude error.

5. (Original) The circuit according to claim 1 further including resistor means coupled to input of the digital reconstruction filter for binary weighting the digital recombined signal produce a downconverted signal is unaffected by resistor tolerance.

6. (Original) A method of image rejection processing of a received RF signal, comprising:

performing downconversion of the received RF signal to produce analog I and Q signals; and

for each of the analog I signal and the analog Q signal:

oversampling the analog signal to obtain an oversampled digital signal;

producing a periodic oversampled digital reference signal; and

logically combining the digital signal with the digital reference signal to produce an image-canceled digital baseband signal.

7. (Original) The method of claim 6, comprising:

converting the digital baseband signal to an analog baseband signal.

8. (Previously presented) An image reject circuit apparatus comprising:

a first frequency downconversion circuit employing a first local oscillator for downconverting in-phase and quadrature signal components of a digitized communication signal to a first intermediate frequency;

sigma delta converters for generating an in phase digital bit stream and a quadrature phase digital bit stream;

a digital in-phase and quadrature phase second local oscillator;

mixing circuitry for mixing respective single serial digital bit stream in-phase signal and single serial digital bit stream quadrature phase signal through a set of logic gates to produce a digital representation of downconverted in-phase and quadrature components;

weighting resistances in series with the outputs of the logic gates for combining the digital representation of the downconverted in-phase and quadrature components according to a value in an in-phase signal and in a quadrature phase signal; and

reconstruction filters to recover in-phase and quadrature phase baseband signals from said downconverted in-phase and quadrature components substantially free of image artifacts.

9. (Original) The image reject circuit apparatus according to claim 8 wherein said mixing circuitry comprises, for each significant bit:

first and second exclusive-OR gates coupled to receive as first input an in phase digital bit stream and as second inputs a high accuracy sine function bit stream and a high accuracy cosine function bit stream;

third and fourth exclusive-OR gates coupled to receive as first input a quadrature phase digital bit stream and as second inputs a high accuracy sine function bit stream;

first OR gate for logically adding the outputs of the first and second XOR gates for the in-phase channel;

first AND gate for logically multiplying the outputs of the first and second XOR gates for the in-phase channel;

second OR gate for logically adding the outputs of the third and fourth XOR gates for the quadrature phase channel; and

second AND gate for logically multiplying the outputs of the third and fourth XOR gates for the quadrature phase channel.

10. (Original) The circuit apparatus according to claim 9 wherein the reconstruction filter comprises:

weighting resistors for each output of each of the first and second AND gates and first and second OR gates, said weighting resistors defining a binary weight for its corresponding bit;

a first lowpass filter means at a first combining node of the first AND gate and first OR gate;

a second lowpass filter means at a second combining node of the second AND gate and second OR gate;

wherein each said weighting resistor of the in-phase channel is connected to said first lowpass filter; and

wherein each said weighting resistor of the quadrature phase channel is connected to said second filter

to yield respective analog I and Q channel signals at baseband.